WEST

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IBM Technical Disclosure Bulletins

Term: (fail$4 or err$7 or defect$3 or fault$3 or bug$4) near2 (address$3 or location) near (compress$5 or de$1compress$4 or compac$6 or hash$4)

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

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Search History

DATE: Tuesday, September 24, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L13	(read$4 or access$4 or load$4 or transfer$4 or shift$4) same (cell or memory or array) same (match$4 or compar$7) and (un$1compressed or compress$ or de$1compress$4 or compact$4) near address same (temporary) and (portion or part) near2 (fail$4 or err$7 or defect$3 or fault$3 or bug$4)	0	L13
L12	(read$4 or access$4 or load$4 or transfer$4 or shift$4) same (cell or memory or array) same (match$4 or compar$7) same (un$1compressed or compress$ or de$1compress$4 or compact$4) near address same (temporary) same (portion or part) near2 defective	0	L12
L11	accessing same (cells or memory array) same (match$4 or compar$7) same (un$1compressed or compress$ or de$1compress$4 or compact$4) near address same (temporary) same (portion or part) near2 defective	0	L11
L10	('US 6138254A')[ABPN1,NRPN,PN,TBAN,WKU]	1	L10
L9	('5363382')[ABPN1,NRPN,PN,TBAN,WKU]	2	L9
L8	('6138254'| '5910921')[ABPN1,NRPN,PN,TBAN,WKU]	4	L8
L7	('6138254')[ABPN1,NRPN,PN,TBAN,WKU]	2	L7
L6	l5 and (fail$4 or err$7 or defect$3 or fault$3 or bug$4) near2 (address$3 or location) near (compress$5 or de$1compress$4 or compac$6 or hash$4) same (spare or memory or array or map$4) same (replac$7 or sub$1stitut$4 or extract$4) same (compar$6 or match$3 or test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) same (read$4 or access$4 or load$4 or transfer$4 or shift$4)	0	L6
L5	(fail$4 or err$7 or defect$3 or fault$3 or bug$4) near2 (address$3 or location) near (compress$5 or de$1compress$4 or compac$6 or hash$4)	38	L5
L4	(fail$4 or err$7 or defect$3 or fault$3 or bug$4) near2 (address$3 or location) same (compress$5 or de$1compress$4 or compac$6 or hash$4) same (spare or memory or array or map$4) same (replac$7 or sub$1stitut$4 or extract$4) same (compar$6 or match$3 or test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) same (read$4 or access$4 or load$4 or transfer$4 or shift$4)	12	L4
L3	('6138254'| '6085334')[ABPN1,NRPN,PN,TBAN,WKU]	4	L3
L2	defect$4 near2 (address$3 or location) same (compres$5 or de$1compres$4 or compac$6 or hash$4) same spare same (memory or array or map$4) same (replac$7 or sub$1stitut$4)	2	L2
L1	defect$4 near2 (address$3 or location) same (compres$5 or de$1compres$4 or compac$6) same spare same (memory or array or map$4) same (replac$7 or sub$1stitut$4)	2	L1

END OF SEARCH HISTORY

WEST

Generate Collection

L5: Entry 9 of 38 File: USPT Sep 12, 2000

DOCUMENT-IDENTIFIER: US 6119251 A
TITLE: Self-test of a memory device

Detailed Description Text (56):
FIG. 9A illustrates an embodiment of a failed address queue according to the present invention for storing failed addresses in a compressed form. In this embodiment, address change detection circuitry 900 detects whether a new failed address in column address latch 210 is the same as the failed address previously stored in the column failing address register 910. If the addresses are not the same, the error detect signal pulse is passed through AND gate 906, causing the new failed address to be written into register 910 and the previously stored failed address to be written into register 912. In this manner, identical failing column addresses are not redundantly stored in the failing address registers.

Detailed Description Text (59):
FIG. 9B illustrates an alternate embodiment of a failed address queue according to the present invention for storing failed addresses in a compressed form. In this embodiment, address change detection circuitry 920 is similar to address change detection circuitry 900 except that OR gate 904 is replaced with NOR gate 922. Address detection circuitry 920 detects whether a new failed address in column address latch 210 is the same address previously stored in the column failing address register 910. If the addresses are the same, the EDS signal passes through AND gate 906, incrementing counter 924. In this manner, the number of identical failing column addresses can be saved without independently storing each failing address in a separate register. If multiple fails are detected at the same column address, the column is given a high priority for replacement with a redundant column (i.e., the column is called a "must" repair column).

5910921

5854796

L5: Entry 9 of 38 File: USPT Sep 12, 2000

DOCUMENT-IDENTIFIER: US 6119251 A
TITLE: Self-test of a memory device

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L5: Entry 18 of 38 File: USPT Nov 8, 1994

DOCUMENT-IDENTIFIER: US 5363382 A
TITLE: Fault analysis apparatus for memories having redundancy circuits

Brief Summary Text (9):
According to the memory fault analysis apparatus of the present invention and having the configuration described above, the address allocation means performs address allocation, that is, address compression for the fault analysis memory so that a plural number of memory cells of the MUT correspond on the basis of a predetermined rule to one of the memory cells of the fault analysis memory, when at least one memory cell of the plural number of memory cells is faulty, there is the write of fault information to the memory cell corresponding to the fault analysis memory. By performing address compression, the size of the area necessary for the FAM becomes smaller than that required in the conventional apparatus and by this it is possible to reduce the judgment time for fault recovery.

Brief Summary Text (10):
According to the present invention as has been described above, performing address compression by the fault analysis memory enables the capacity of the FAM to be reduced and also enables the time required to judge fault recovery to be shortened.